Abstracts

Gigabit Logic Prospects of GaAs E-JFET Integrated Circuits

R. Zuleeg, J.K. Notthoff and A.F. Behle. "Gigabit Logic Prospects of GaAs E-JFET Integrated Circuits." 1979 MTT-S International Microwave Symposium Digest 79.1 (1979 [MWSYM]): 512-515.

Computer simulation and experimental results will be presented for a 1 mu m GaAs enhancement mode JFET. Logic performance of 250 ps propagation delay time with a power dissipation of 200 mu W/gate at a fan-out of 3 offers gigabit logic for LSI, i.e. delay-power product of 50 fJ. A planar integration will be described which utilizes selective ion implantation of n- and p- impurities for the channel and pn-junction gate formation in semi-insulating GaAs substrate material.

❑ Return to main document.